(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication: 13.06.2001 Bulletin 2001/24

- (51) Int CI.⁷: **C30B 25/12**, C23C 16/458, C30B 31/14
- (21) Application number: 00311016.0
- (22) Date of filing: 11.12.2000
- (84) Designated Contracting States:

 AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU

 MC NL PT SE TR

 Designated Extension States:

 AL LT LV MK RO SI
- (30) Priority: 10.12.1999 US 459313
- (71) Applicant: Applied Materials, Inc. Santa Clara, California 95054 (US)
- (72) Inventors:
 - Yudovsky, Joseph Cambell, California 95008 (US)
 - Lei, Lawrence C.
 Milpitas, CA 95035 (US)

- Umotoy, Salvador Antioch, California 94509 (US)
- Madar, Thomas A.
 Sunnyvale 94089 (US)

(11)

- Dixit, Girish San Jose, California 95135 (US)
- Tzu, Gwo-Chuan Sunnyvale, California 94086 (US)
- (74) Representative: Draper, Martyn John et al Boult Wade Tennant Verulam Gardens 70 Gray's Inn Road London WC1X 8BT (GB)

(54) Self aligning non contact shadow ring process kit

(57) The invention provides a removable first edge ring configured for pin and recess/slot coupling with a second edge ring disposed on the substrate support. In one embodiment, a first edge ring includes a plurality of pins, and a second edge ring includes one or more alignment recesses and one or more alignment slots for mating engagement with the pins. Each of the alignment recesses and alignment slots are at least as wide as the corresponding pins, and each of the alignment slots extends in the radial direction a length that is sufficient to compensate for the difference in thermal expansion between the first edge ring and the second edge ring.

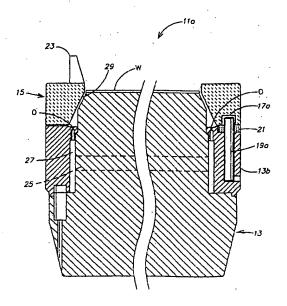


FIG. 2

Description

[0001] The present invention relates to an improved susceptor which inhibits the deposition of process gasses on the edge and backside of a substrate, and which may be easily removed and cleaned.

[0002] Chemical vapor deposition (CVD) is one of a number of processes used to deposit thin films of material on semiconductor substrates. To process substrates using CVD, a vacuum chamber is provided with a susceptor configured to receive a substrate. In a typical CVD chamber, the substrate is placed into and removed from the chamber by a robot blade and is supported by a substrate support during processing. A precursor gas is charged into the vacuum chamber through a gas manifold plate situated above the substrate, where the substrate is heated to process temperatures, generally in the range of about 250° to 650° C. The precursor gas reacts on the heated substrate surface to deposit a thin layer thereon and to form volatile byproduct gases, which are pumped away through the chamber exhaust system.

[0003] A primary goal of substrate processing is to obtain the largest useful surface area, and as a result the greatest number of chips, possible from each substrate. This is highlighted by the recent demands from semiconductor chip manufacturers to minimize edge exclusion on the substrates processed, so that as little of the substrate surface as possible, including the edge of the wafer, is wasted. Some important factors to consider include processing variables that affect the uniformity and thickness of the layer deposited on the substrate, and contaminants that may attach to the substrate and render all or a portion of the substrate defective or useless. Both of these factors should be controlled to maximize the useful surface area for each substrate processed.

[0004] One source of particle contamination in the chamber is material deposited at the edge or on the backside of the substrate that flakes off or peels off during a subsequent process. Substrate edges are typically beveled, making deposition difficult to control over these surfaces. Thus, deposition at substrate edges is typically nonuniform and, where metal is deposited, tends to adhere differently to a dielectric than to silicon. If a wafer's dielectric layer does not extend to the bevel, metal may be deposited on a silicon bevel and eventually chip or flake, generating unwanted particles in the chamber. Additionally, chemical mechanical polishing is often used to smooth the surface of a substrate coated with tungsten or other metals. The act of polishing may cause any deposits on the edge and backside surfaces to flake and generate unwanted particles.

A number of approaches have been employed to control the deposition on the edge of the substrate during processing. One approach employs a shadow ring which essentially masks a portion of the perimeter of the substrate from the process gasses. One disadvantage

with the shadow ring approach is that, by masking a portion of the substrate's perimeter, the shadow ring reduces the overall useful surface area of the substrate. This problem is made worse if the shadow ring is not accurately aligned with the substrate, and alignment can be difficult to achieve..

[0005] Another approach employs a purge ring near the edge of the substrate for delivering a purge gas along the substrate's edge to prevent edge deposition. The purge gas limits or prevents the deposition gas from reaching the substrate and thus limits or prevents deposition on the wafer's beveled edge. A third approach uses a shutter ring and a purge ring in combination to form a purge gas chamber having a purge gas inlet and outlet adjacent the substrate's edge so as to guide the purge gas across the wafer's edge.

[0006] A wafer typically sits inside (radially) the purge ring, with a gap therebetween. Conventionally, purge rings are made of aluminum and are welded to the substrate support in an effort to prevent the ring from deforming during processing. However, during the thermal cycling which occurs within a CVD processing chamber, the aluminum rings nonetheless deform, losing the integrity of their shape and therefore compromise their ability to keep particles from depositing on the substrate's edge. This can change the size of the gap, leading to non-uniformity of deposition across the wafer's edge. As the aluminum rings expand and contract, material thereon can flake, and create particles which can contaminate the wafer.

[0007] Further, in order for the rings to work effectively for shadowing and/or for purging, they must be frequently cleaned to remove deposition material which can alter the gap or flake off and contaminate the wafer. Such cleaning increases chamber downtime, reduces throughput and results in higher operating costs.

[0008] Accordingly a need exists for an improved susceptor which can reliably prevent edge deposition, and which can be easily cleaned.

[0009] In one aspect, the present invention overcomes the problems of the prior art by providing a substrate support having a removable edge ring, which may be made of a material having a lower coefficient of thermal expansion (CTE) than that of the substrate support.
The edge ring may be a shadow ring, a purge ring, or

function as both edge ring and shadow ring. The edge ring and the substrate support are configured for pin and slot coupling. In one aspect, either the edge ring or the substrate support includes a plurality of pins, and the other of the edge ring or the substrate support includes a plurality of alignment slots in which the pins may be inserted. Each of the slots is at least as wide as a corresponding one of the plurality of pins and extends in the radial direction. a length that is sufficient to compensate for the difference in thermal expansion between the substrate support and the edge ring.

[0010] In another aspect, the invention provides a removable first edge ring positioned above the substrate

20

support and configured for pin and slot coupling with a second edge ring attached to the substrate support. Preferably, either the first edge ring or the second edge ring includes a plurality of pins, and the other of the first edge ring or second edge ring includes one or more alignment recesses and one or more alignment slots. The pins are inserted into the alignment recesses and alignment slots to couple the two edge rings in alignment. Each of the alignment recesses and alignment slots are at least as wide as the corresponding one of the plurality of pins, and each of the alignment slots extends in the radial direction a length that is sufficient to compensate for the difference in thermal expansion between the first edge ring and the second edge ring.

[0011] Other objects, features and advantages of the present invention will become more fully apparent from the following detailed description of the preferred embodiments, the appended claims and the accompanying drawings.

FIG. 1 is an exploded perspective view of a susceptor of the invention;

FIG. 2 is a side view, in pertinent part, of a susceptor of the invention;

FIG. 3 is a side view, in pertinent part, of a susceptor 25 of the invention:

FIG. 4 is a side view in pertinent part of a susceptor of the invention;

FIGS. 5A and 5B are side views in pertinent part of a susceptor of the invention;

FIG. 6 is a side view in pertinent part of a susceptor of the invention:

FIG. 7 is a side view of a chamber showing a susceptor of the invention in a non-processing position. FIG. 8 is a top view of a shadow ring of the invention; FIG. 9 is a top view of a shadow ring supported on a chamber body ring of the invention;

FIG. 10 is a side view of a chamber showing a susceptor of the invention- in a processing position; and FIG. 11 is a side view of a chamber showing a susceptor of the invention.

[0012] FIG. 1 is an exploded perspective view of a susceptor 11a. The susceptor 11a comprises a substrate support 13, adapted for pin and slot coupling with an edge ring, such as purge ring 15. Specifically, the substrate support 13 comprises three pins 19a-c which extend upwardly from the top surface of substrate support 13. The bottom surface of the purge ring 15 comprises three alignment slots 17a-c positioned to interface with the three pins 19a-c. The substrate support 13 comprises a central wafer supporting surface 13a, and the three pins 19a-c are disposed substantially equally spaced around the substrate supporting surface 13a. Each of the slots 17a-c is at least as wide as the corresponding pin 19a-c, and extends radially outward from the center of the substrate supporting surface 13a, in the direction in which the substrate support 13 expands

and contracts during thermal cycling.

[0013] The substrate support 13 is preferably made of a metal such as aluminum, as is conventional. The purge ring 15 is generally made of a mat rial having a lower coefficient of thermal expansion (CTE) than the CTE of the substrate support 13 material. Preferably the purge ring 15 is made of a ceramic material. The slots 17a-c extend a length which is sufficient to compensate for the difference in thermal expansion between the substrate support 13 and the purge ring 15, over the range of process temperatures to which the susceptor 11 a is exposed. This difference in thermal expansion may be due to the different CTE of the purge ring 15 material and the substrate support 13 material. Preferably each pin 19a-c is surrounded by a pad 21 made of a thermally insulating material, so as to achieve thermal insulation between the substrate support 13 and the purge ring 15, as further described below with reference to FIG. 2. The pads 21 are preferably made of a highly polished ceramic and therefore allow the purge ring 15 to slide easily therealong while minimizing particle generation. The purge ring 15 may further include a plurality of wafer guide pins 23 to facilitate accurate wafer placement, as is disclosed in U.S. Patent Application Serial No. 09/103,462 filed June 24,1998 (incorporated herein in its entirety).

[0014] FIG. 2 is a side view, in pertinent part, of a susceptor 11a, having a wafer W positioned thereon. As shown in FIG. 2 the substrate support 13, the purge ring 15 and the slots 17a-c are configured such that with use of the pad 21, no direct contact exists between the substrate support 13 and the purge ring 15. By thermally insulating the purge ring 15 from the metal substrate support 13, the purge ring 15 experiences less thermal stress then would otherwise result if the purge ring 15 were to directly contact the typically higher temperature substrate support 13. Also as shown in FIG. 2, the slot 17a has a depth greater than the length of the pin 19a to reduce thermal conduction from the substrate support 13 to the purge ring 15, via the pin 19a.

[0015] The slots 17a-c extend radially outward relative to the center of the substrate support 13 and preferably are each just slightly wider than the respective pin 19a-c. This prevents the purge ring 15 movement laterally relative to the substrate support occuring as a result of thermal cycling induced expansion and contraction from being more than the maximum distance allowing clearance between the slot 17a and the pin 19a pair. The pins 19a-c also restrict rotational movement of the purge ring 15 relative to the substrate support 13, thereby providing rotational alignment.

[0016] The substrate support 13 comprises a purge gas delivery channel 25 and a diffuser ring 13b which couples purge gas from the purge gas delivery channel 25 through a purge gas distribution channel 27 defined by an inner edge of the diffuser ring 13b and an outer edge of the substrate support 13, and then through a plurality of small orifices O formed in the diffuser ring

13b to a lower edge of the purge ring 15.

[0017] In operation the wafer W is positioned on the wafer supporting surface 13a such that the edge of the wafer W is positioned adjacent the outlet of the purge slot 29. In this manner as purge gas flows upwardly through the purge slot 29 along the edge of the wafer W, deposition on the wafer's edge is prevented. During a deposition process, the susceptor 11a is typically heated to a temperature in the range of 350° to 475°C, typically by a heating coil embedded in or contacted with the underside of, the susceptor 11a. However, for chamber maintenance or cleaning, the susceptor 11a is typically allowed to cool back to ambient temperatures.

[0018] This temperature change causes thermal expansion and contraction of the chamber elements, including the substrate support 13 and the purge ring 15. Despite thermal cycling which occurs during CVD processing, and the resulting expansion and contraction of the substrate support 13 and the diffuser ring 13b, thermally induced stresses are not imposed upon the purge ring 15, as it (and the pins 19a-c supporting it) can move radially as the temperature changes, due to the pin 19a-c and slot 17a-c coupling. Any thermally induced expansion of the gap between the purge ring 15 and the wafer W is insignificant. Accordingly edge deposition is more uniformly and reliably prevented. Moreover, the purge ring 15 may be easily lifted off the pins 19a-c for routine cleaning or replacement. Accordingly downtime is minimized.

[0019] FIG. 3 is a side view, in pertinent part, of a susceptor 11b. The inventive susceptor 11b of FIG. 3 is similar to the susceptor 11a of FIG. 2, except the substrate support 13 of FIG. 2 does not comprise the diffuser ring 13b. Instead, the purge gas delivery channel 25 delivers purge gas to a purge gas distribution channel 27 which is defined by an inner edge of the purge ring 15 and an outer edge of the substrate support 13, as is the more narrowly defined purge gas slot 29. The embodiment of FIG. 3 requires fewer parts, and replaces the orifices O (of FIG. 1) with a restrictor gap R. The restrictor gap R is formed by a horizontal notch in the substrate support 13 and a corresponding horizontal protrusion in the purge ring 15. The size of the restrictor gap R is determined by the respective vertical dimensions of the substrate support 13 and the purge ring 15 to the horizontal notch or protrusion, and by the thickness of the pad 21. The embodiment of FIG. 3 reduces clogging because the restrictor gap R which expands radially around the substrate support 13 in a continuum is less likely to clog than are the plurality of orifices . By reducing the number of parts, the FIG. 3 embodiment also reduces the probability of differential expansion therebetween and the resultant particle generation. Note that, like the FIG. 1 and 2 embodiment, the purge ring 15 rests on the insulator pads 21 and is aligned by the pins 19.

[0020] FIG. 4 is a side view, in pertinent part, of a susceptor 11c. As shown in FIG. 4, the purge ring 15 of the inventive susceptor 11 c has a plurality of pins 19 (only

one shown) which extend downward from the bottom surface of the purge ring 15. The pins 19 are pressed into the purge ring 15 and the pads 21 are secured to the pins 19 in the same manner, or maybe integral to the pins 19. In operation, each pin 19 is inserted within a corresponding slot 17 located on the substrate support 13. In this example the slots 17 are formed in the diffuser ring portion 13b of the substrate support 13. Thus, FIG. 4 shows that the positions of the pins 19 and the slots 17 may be switched, and still achieve the advantages of pin and slot coupling.

[0021] FIGS. 5A and 5B are side views, in pertinent part, of a susceptor 11d. The purge ring 15a of FIGS. 5A and 5B is configured such that the inner edge 15a overhangs the edge of the wafer W. Thus, the purge ring 15a functions as both a purge ring 15a and a shadow ring 4 (overhanging or shadowing the wafer's edge). The pin and slot coupling of FIGS. 5A and 5B allows the substrate support 13 to expand and contract without affecting the shape or position of the purge ring 15a, as described above with reference to FIGS, 2 and 3, FIG, 5A shows the purge ring 15a in a process position, and FIG. 5B shows the purge ring 15a in a wafer W transfer position. Because shadow rings 4 overlap the wafer's edge, they are conventionally supported in a wafer W transfer position above the substrate support 13 (e.g., by a hanger or lip which protrudes from the chamber wall) while a wafer W is placed on or extracted from the substrate support 13. After a wafer W is placed on the substrate support 13, the substrate support 13 elevates and engages the bottom of the shadow ring 4, transferring the shadow ring 4 from the lip to the substrate support 13 as further described below.

[0022] Conventional substrate supports 13, whether to be used with a purge ring 15 and/or shadow ring 4, are initially lowered to a wafer W transfer position. A wafer handler then carries a wafer W into position above the substrate support 13 and the lift pins (not shown) lift the wafer W off the wafer handler. Thereafter, the wafer handler retracts, and the substrate support 13 is further elevated to engage the shadow ring 4.

[0023] FIG. 6 is a side view in pertinent part of a susceptor 11e. The inventive susceptor 11e is configured to facilitate access to the purge gas distribution channel 25 for cleaning. Specifically, the surface of the substrate support 13 in which the pin 19 (or in an alternative embodiment, the slot 17) is located, is below the outlet of the purge gas distribution channel 25. Thus, when the purge ring 15 and/or shadow ring 4 is removed from the substrate support 13, the gas distribution channel's outlet is exposed. To further facilitate cleaning, the purge gas distribution channel 25 may be angled upwardly (preferably between 0° and 30°), as shown in FIG. 6.
[0024] FIG. 7 is a side view of a chamber showing a susceptor 11f of the invention in a lowered non-process-

susceptor 11f of the invention in a lowered non-processing position. The susceptor 11f comprises a removable first edge ring, such as a shadow ring 4, supported by a chamber body ring 200 disposed on the internal sur-

face 102 of the processing chamber body 100 above the substrate support 13 and a second ring, such as a purge ring 15, disposed on the substrate support 13. The purge ring 15 may be attached to the substrate support 13 as described above relating to Figs 1-6. The substrate support may be made of various materials, such as aluminum and ceramic, and may include a heating element, such as a resistive heating coil. The shadow ring 4 comprises a plurality of tapered or frustoconically shaped pins 19 (two shown), equally spaced around the perimeter of the shadow ring 4 and extending downwardly therefrom. The purge ring 15 includes at least one tapered or frustoconically shaped alignment recess 5 and at least one tapered or frustoconically shaped alignment slot 6 formed therein. Although the invention is shown and described with a shadow ring having pins thereon and a purge ring having recess/slot thereon, it is understood that invention contemplates embodiments wherein the pin and recess/slot coupling may be disposed on either the shadow ring or the purge ring. The invention also contemplates embodiments wherein either the pins or the recesses/slots include tapered surfaces:

[0025] The pins 19 are positioned to interface with the alignment recess 5 and the alignment slot 6. The alignment recess 5 and the alignment slot 6 are at least as wide as a corresponding one of the plurality of pins 19. in one aspect, the width is defined as the dimension perpendicular to the radial direction, relative to the center of the purge ring 15. Referring to Figure 8, which is a top view of a purge ring 15 of the invention showing the alignment recess 5 and the alignment slot 6, line 800 represents the radial direction relative to the center of the purge ring 15, and line 802 represents the direction perpendicular to the radial direction relative to the center of the purge ring 15. The width of the alignment slot 6, being the dimension perpendicular to the radial direction relative to the center of the purge ring 15, is shown by segment 804. The radial dimension of the alignment slot 6 is shown by segment 806. The alignment slot 6 extends in a radial direction, relative to the center of the purge ring 15, a length that is sufficient to compensate for any difference in thermal expansion between the purge ring 15 and the shadow ring 4. The radial dimension (i.e., length) of the alignment slot 6 is up to about sixty mils greater, preferably up to about forty mils greater, than the radial dimension of the corresponding pin 19. The width of the alignment recess 5 and alignment slot 6 is between about three mils and about ten mils wider, preferably between about three mils and about eight mils wider, than the width of the corresponding pin 19. The coupling of the pins 19 with the alignment recess 5 and the alignment slot 6 restricts movement of the shadow ring 4 caused by thermal cycling induced expansion and contraction or other causes to less than the length of the alignment slot 6. The pins 19 also restrict rotational movement of the shadow ring 4 relative to the purge ring 15, thereby providing rotational alignment.

[0026] The pins 19 as shown in FIG. 7 preferably have a frustoconical shape, tapering from a base portion to a top portion. The alignment recess 5 and the alignment slot 6 have matching tapering sidewalls forming a wider opening portion and a narrower bottom portion for receiving the tapered pins 19. This configuration allows for and corrects gross misalignment between the two rings because the narrower tip portion of the pins 19 can be inserted into the wider opening portion of the recess 5 and slot 6 with a greater margin of misalignment. Thus, with frustroconically shaped or tapered pins 19 instead of nontapering (i.e., cylindrical) pins, recess 5, and slot 6. misalignment of the shadow ring 4 with the purge ring 15, due to thermal expansion or other causes can be corrected when the pins 19 are inserted into the recess 5 and slot 6 when the rings come together. As the pins 19 are inserted into the recess 5 and slot 6, misalignment between the shadow ring and the purge ring is corrected as the surface of the pin 19 slides along the surface defined by the recess 5 or slot 6. The two rings are aligned as the pins 19 are fully inserted into the recess

[0027] The pin 19 and recess 5/slot 6 coupling allows the shadow ring 4 to move with respect to the purge ring 15 due to different thermal expansions between the two rings without imposing stresses on either ring that could cause ring deformation, flaking or breakage of any of the components. The shadow ring 4 remains in pivotal alignment to the purge ring 15 at the location of the pin 19 and recess 5 coupling, while the pin 19 and slot 6 coupling allows the shadow ring to move slightly (i.e., restricted by the length of the slot 6) relative to each other due to different thermal expansions between the two rings. The invention provides consistent alignment of the shadow ring 4 with the purge ring 15 and the substrate. Moreover, the shadow ring 4 may be easily removed for cleaning or replacement. Down time is thereby minimized.

[0028] FIG. 9 is a top view of a shadow ring 4 supported on a chamber body ring 200. A chamber body ring 200 is secured to the internal surface 102 of the chamber body 100. The chamber body ring 200 includes a plurality of recesses 202 formed in the upper portion of the internal surface 220 of the chamber body ring 200. The shadow ring 4 includes a plurality of projections 10 configured to rest on the surface of the chamber body ring 200 defined by the recesses 202. Preferably, four projections 10 are spaced equally along the perimeter of the shadow ring 4. When not coupled to the purge ring 15, the shadow ring 4 may be supported by the chamber body ring 200 via the projections 10 resting on the surface of the recesses 202. The recesses 202 are sized to allow for thermal expansion of the shadow ring 4, and yet keep the shadow ring 4 sufficiently aligned with the purge ring 15 so that the pins 19 stay within the capture range of the recess 5 and slot 6. The sidewall surfaces of the recess 202 may also be tapered to urge a shadow ring 4 into the desired aligned position on the

chamber body ring 200.

[0029] FIG. 10 is a side view of a chamber showing a susceptor 11f in a processing position. As shown, the purge ring 15 attached to the substrate support 13 contacts and lifts the shadow ring 4. The pins 19 of the shadow ring 4 are inserted into the recess 5 and slot 6 of the purge ring 15. The shadow ring 4 is thereby lifted off the chamber body ring 200, so that the projections 10 of the shadow ring 4 are lifted off the internal surface 220 of the chamber body ring 200 defined by the recesses 202. In this configuration, the shadow ring 4 is positioned about 3 to 5 millimeters above a wafer W and overhangs a portion of the perimeter, or edge, of the wafer W, preventing deposition thereon during CVD processing.

[0030] In operation, the substrate support 13 is initially lowered to a wafer transfer position, as shown in FIG. 7. A wafer handler comprising a robot blade then carries a wafer into position above the substrate support 13. Lift pins (not shown) lift the wafer W off the robot blade, and the robot blade retracts. The substrate support 13 is elevated to position the substrate thereon, and then the substrate support 13 further elevates so that the purge ring 15 attached thereto lifts the shadow ring 4 off the chamber body ring 200, as shown in FIG. 10. As the purge ring 15 engages the shadow ring 4, the pins 19 are inserted into the alignment recess 5 and alignment slot 6. The tapered surfaces of the pins 19 slides along the tapered surfaces of the alignment recess 5 and alignment slot 6, urging the shadow ring 4 into desired alignment with the purge ring 15.

[0031] FIG. 11 is a side view of a chamber showing a susceptor 11 g in a non-processing configuration. In this aspect of the invention, the substrate support 13 includes a ceramic susceptor and a ceramic purge ring 15 disposed thereon. The purge ring 15 and the shadow ring 4 include the pin and slot/recess coupling of the invention as described above.

[0032] As is apparent from the above description, a chamber such as the chamber described in commonly assigned U.S. Patent Application Serial No. 09/103,462, filed June 24, 1998 (incorporated in its entirety), when employing the inventive susceptor of FIGS. 1 through 5, provides superior edge deposition prevention and increased throughput as compared to conventional deposition chambers (CVD, PVD, etc.).

[0033] The foregoing description discloses only the preferred embodiments of the invention, modifications of the above disclosed apparatus and method which fall within the scope of the invention will be readily apparent to those of ordinary skill in the art. For instance, the inventive susceptor comprises pin and slot coupling between any type of edge ring (purge ring and/or shadow ring), whether the pins are located on the substrate support or the ring. Although each of the figures shows the use of thermally insulating pads these pads are optional. Further, it will be understood that a heating element may be included in the susceptor, as is conventionally known. Also as conventionally known, each of the purge

gas delivery channels 25 of the various embodiments of the invention preferably open into a purge gas distribution channel 27 which also extends somewhat below the opening of the purge gas delivery channel 25 (as shown in each of the figures), so as to create a buffer channel which ensures more even distribution of the purge gas to the purge slots 29.

[0034] The terms pin and slot are to be broadly interpreted to include shapes other than straight pins and slots 6 (e.g., rectangular keys, etc.). Further, purge ring or purge ring/shadow ring can be advantageously removably coupled to a substrate support, by mechanisms other than pin and slot coupling. Any removably coupled purge ring will benefit from the exposed outlet of the purge gas delivery channel and the upwardly angled purge gas delivery channel. Similarly a susceptor whether or not having a removably coupled purge ring, can benefit from the definition of a purge gas distribution channel having a restrictor gap between the substrate support and the purge ring. Thus, these aspects of the invention should not be respectively limited to pin and slot coupling or to removably coupled purge rings.

25 Claims

30

- 1. An apparatus comprising:
 - a) a substrate support;
 - b) a first edge ring disposed on the substrate support, the first edge ring having one or more tapered recesses; and
 - c) a second edge ring having one or more matching tapered pins for mating engagement with the one or more tapered recesses of the first edge ring.
- The apparatus of claim 1, wherein the first edge ring includes one or more slots disposed for mating engagement with the one or more tapered pins on the second edge ring.
 - The apparatus of claim 1 or claim 2, wherein the first edge ring comprises a purge ring.
 - The apparatus of any preceding claim, wherein the second edge ring comprises a shadow ring.
 - 5. The apparatus of any preceding claim, wherein the first edge ring includes one tapered recess and one diametrically positioned tapered slot, and wherein the second edge ring includes two tapered pins diametrically positioned for mating engagement with the recess and the slot.
 - **6.** The apparatus of claim 3, wherein the substrate support comprises a purge gas channel.

10

- An apparatus for processing substrates, comprising; a chamber and an apparatus according to any preceding claim disposed in the chamber.
- 8. The apparatus of claim 7, further comprising: a chamber body ring disposed on an interior surface of the chamber, the chamber body ring having one or more recesses for supporting engagement with the second edge ring.
- The apparatus of claim 8, wherein the one or more recesses on the chamber body ring include tapered side surfaces.
- 10. A method for supporting a substrate in a chamber, comprising:

a) positioning the substrate on a substrate support having a first edge ring disposed around a substrate supporting surface, the first edge ring having one or more recesses; and b) positioning a second edge ring above the first edge ring, wherein the second edge ring includes one or more pins for mating engagement with the one or more recesses on the first edge ring.

- 11. The method of claim 10, wherein the first edge ring includes one or more slots disposed for mating engagement with the one or more pins on the second edge ring.
- **12.** The method of claim 10 or claim 11, wherein the first edge ring comprises a purge ring.
- 13. The method of any of claims 10 to 12, wherein the second edge ring comprises a shadow ring.
- 14. The method of any of claims 10 to 13, wherein the first edge ring includes one tapered recess and one diametrically positioned tapered slot, and wherein the second edge ring includes two tapered pins diametrically positioned for mating engagement with the recess and the slot.
- 15. The method of any of claims 10 to 14, further comprising: flowing a purge gas around the substrate during substrate processing.
- 16. An apparatus comprising a substrate support having a removable edge ring, a plurality of pins provided in one of the edge ring and the substrate support and a plurality of complementary recesses provided on the other of the edge ring and substrate support to locate the edge ring with respect to the support, at least one of the recesses providing an alignment slot which is elongate in a radial direction to allow for movement of the pin within the slot when

the apparatus undergoes the thermal expansion.

- 17. An apparatus according to claim 16, wherein the edge ring has a lower co-efficient of the thermal expansion than that of the substrate support.
- 18. An apparatus according to claim 16 or claim 17, wherein a second edge ring is attached to the substrate support and is provided with the pins or slots as the case may be.

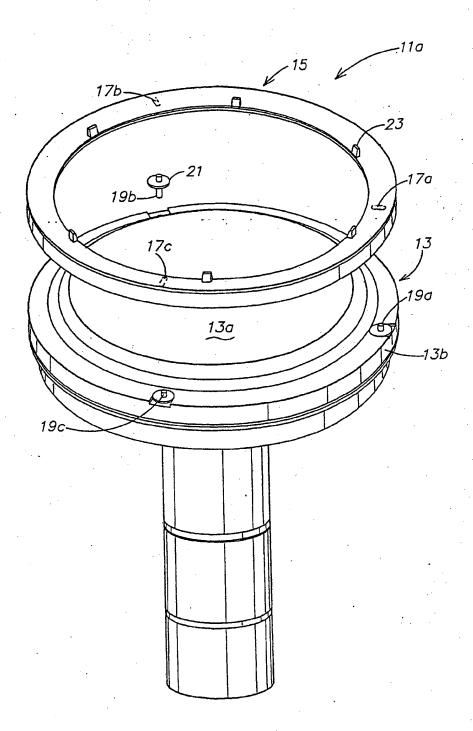


FIG. 1

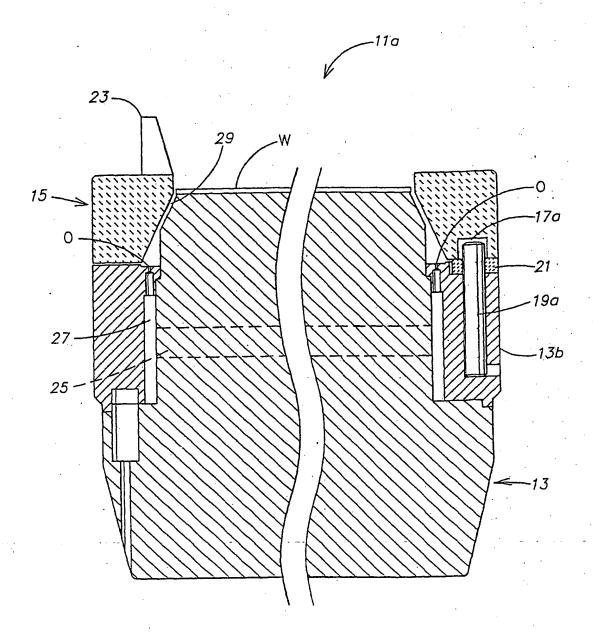


FIG. 2

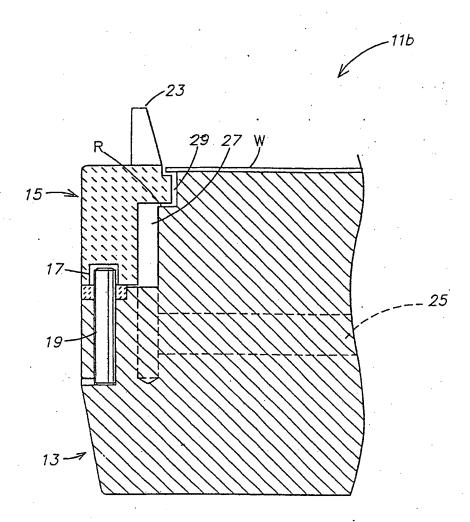


FIG. 3

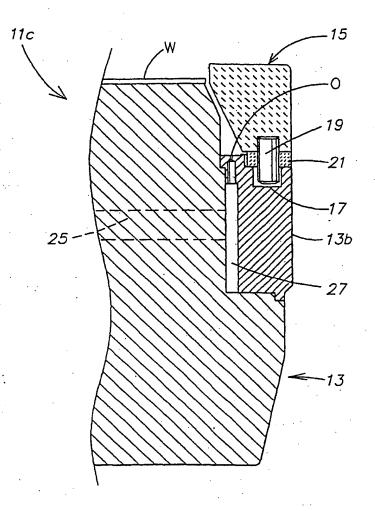


FIG.4

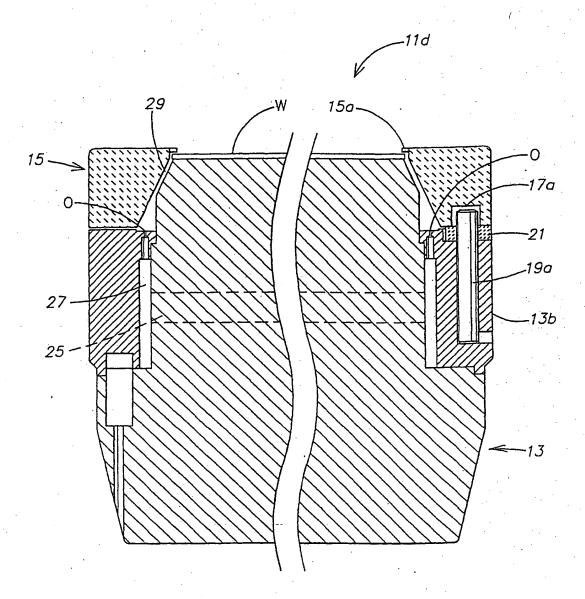


FIG. 5A

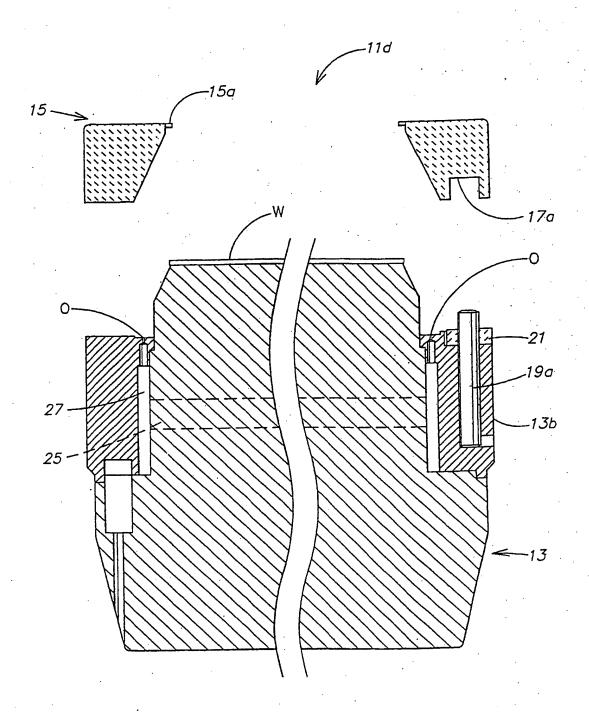


FIG. 5B

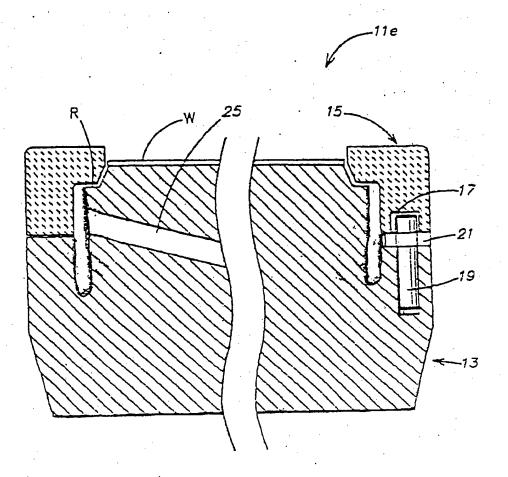
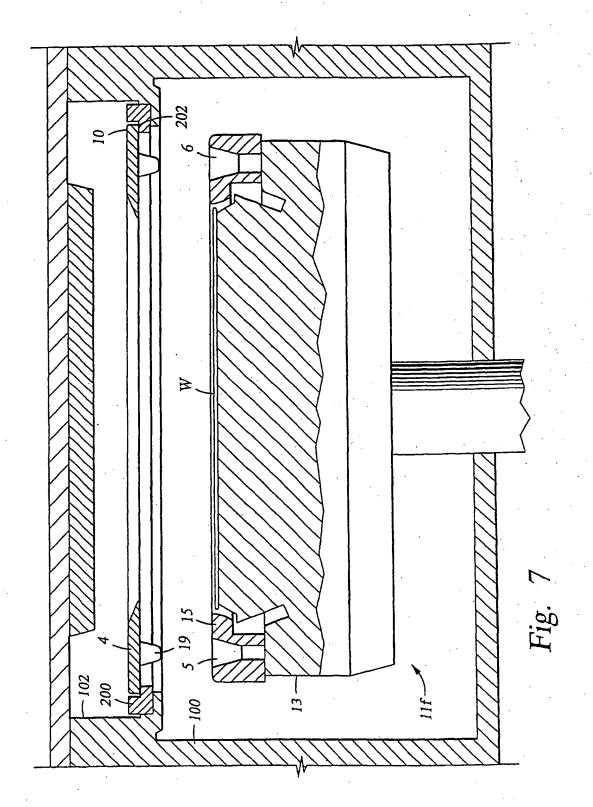


FIG. 6



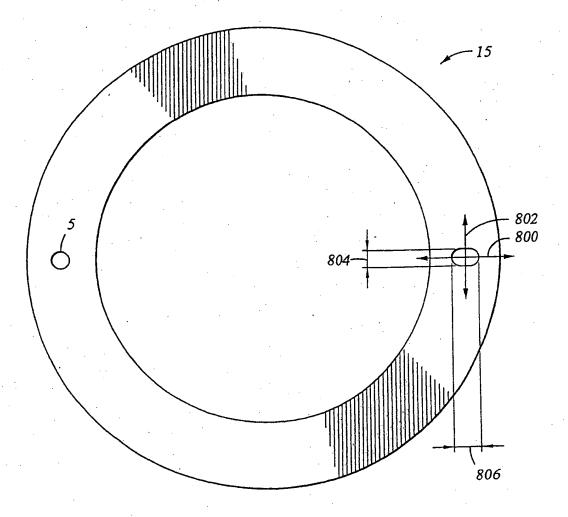


Fig. 8

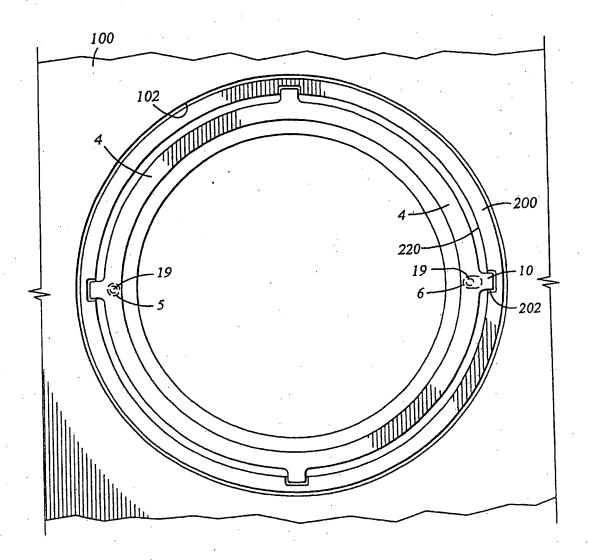
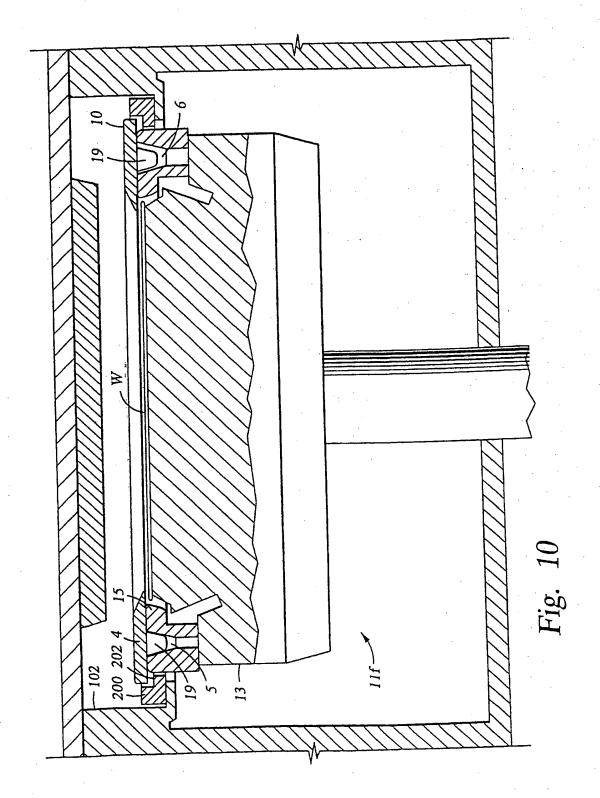
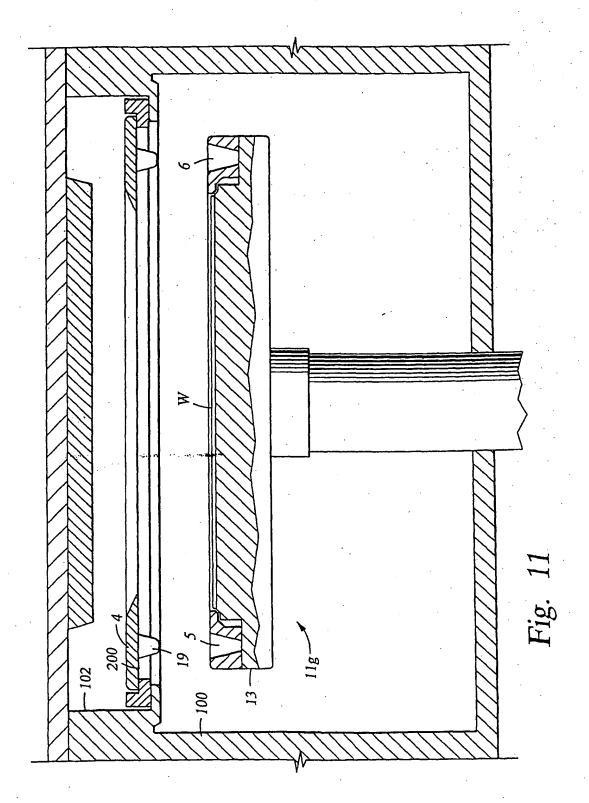


Fig. 9







EUROPEAN SEARCH REPORT

EP 00 31 1016

Category	Citation of document with indica of relevant passages		Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.CI.7)
X	EP 0 698 674 A (NOVELL 28 February 1996 (1996 * column 17, line 35 - figure 11 *	US SYSTEMS INC) -02-28)	1,2,7,	C30B25/12 C23C16/458 C30B31/14
X	US 5 769 951 A (BENZIN 23 June 1998 (1998-06- * column 14, line 22 -	23)	1,2,7,	·
Х	EP 0 553 691 A (APPLIE 4 August 1993 (1993-08 * column 7, line 52 - figures 3,5 *	-04)	1,2,7,	
A	EP 0 688 888 A (APPLIE 27 December 1995 (1995 * column 7, line 41 - figure 3 *	-12-27)	1-18	
A	US 5 888 304 A (UMOTOY 30 March 1999 (1999-03 + column 5, line 65 -	-30)	1-18	TECHNICAL FIELDS SEARCHED (Int.CI.7)
A	US 5 632 873 A (EDWARD 27 May 1997 (1997-05-2			C23C C30B
				·
	The present search report has been	drawn up for all claims		
	Place of search	Date of completion of the search		Examiner C
X : part Y : part doct A : tech	THE HAGUE ATEGORY OF CITED DOCUMENTS icutarly relevant if taken alone icutarly relevant if combined with another ument of the same category incopical beckground —written disclosure		tie underlying the ocument, but publiste in the application for other reasons	Ished on, or

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

EP 00 31 1016

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

21-03-2001

	Patent document ad in search repo		Publication date		Patent family member(s)	Publication date
ΕP	0698674	Α	28-02-1996	US	5578532 A	26-11-1990
C.F	0096074	п	20 02 1770	ÜS	5843233 A	01-12-199
				JP	8191051 A	23-07-199
				US	5769951 A	23-06-1998
				US	5882417 A	16-03-199
	5769951	Α	23-06-1998	US	5843233 A	01-12-199
UJ	3,03301	••		US	5578532 A	26-11-199
				US	5374594 A	20-12-199
	•			US	5230741 A	27-07-199
	•			ΕP	0698674 A	28-02-199
				JP	8191051 A	23-07-199
				ÜS.	5882417 A	16-03-199
				US	5620525 A	15-04-199
	-			ÜS	5925411 A	20-07-199
				DE	69117824 D	18-04-199
				DE	69117824 T	08-08-199
				DE	467623 T	23-07-199
				EP	0467623 A	22-01-199
				ĴΡ	2642005 B	20-08-199
				JP	4233221 A	21-08-199
				KR	9711643 B	12-07-199
				US	5238499 A	24-08-199
	0553691	A	04-08-1993	US	5304248 A	19-04-199
C.T	0553031	n		JP	2641373 B	13-08-199
	•			ĴΡ	7221024 A	18-08-199
				KR	225703 B	15-10-19
				US	5851299 A	22-12-19
				US	5855687 A	05-01-19
	0688888		27-12-1995	US	5476548 A	19-12-19
E1		,,	2. 22 2311	JP	8081775 A	26-03-19
115	5888304	Α	30-03-1999	JP	10041253 A	13-02-19
U	3500304	.,		US	6033480 A	07-03-20
115	5632873	Α	27-05-1997	NON	E	•

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

			en en er verker en
		ra É	
() (1)		*	
	and the second s		
*			
		Harris San	
Francisco de la companya de la comp Performancia de la companya de la c		45 4 7	
		Approximation of the second se	
		in the transfer of the second	
		And the second of the second o	
	and the second of the second o		
		Willy Control of the Control of the	
	and the second s		
			المراجع المستوالين
antana di Kabupatèn Kabupatèn Kabupatèn Kabupatèn Kabupatèn Kabupatèn Kabupatèn Kabupatèn Kabupatèn Kabupatèn Kabupatèn Kabupatèn			and the state of t